Minimizing Power Consumption in Combinational Logic Circuits by Reducing Switching Activity

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Abstract

The aim of the present paper is to investigate the minimization of the power consumption in combinational circuits by reducing the switching activity. A synthesis approach based on an iterative procedure that compares the minterms consequently, eliminate the complementary variables, then ORing all the terms in one simplified equation is introduced . The results show that about 10% reduction in switching activity has been obtained by using this method if it is compared with the normal optimal solution obtained from K-map method.

Key Word: switching activity, low-power consumption, combinational circuits,CMOS circuit , K-map.

تقليل القدرة المستهلكة في الدوائر المنطقية بتقليل فعالية التشغيل

المستخلص

يهدف البحث الحالي الى دراسة تقليل القدرة المستهلكة في الدوائر المنطقية بتقليل فعالية التشغيل . يستند الاسلوب المتبع في البحث على عملية متتابعة يتم فيها مقارنة المدخلات المتشابهه (ذات الخرج ١) واختزال العناصر المتتامة ثم جمع الحدود المبسطة في معادلة واحدة. تشير النتائج الى ان فعالية التشغيل قد تم تقليلها بحدود ١٠% عند استخدام هذه الطريقة بالمقارنة مع تلك الدوائر المصممة باستخدام الطريقة التقليدية في مخطط كارنوف .

1. Introduction

The popularity of small, portable communications and computing devices has contributed to increasing interest in producing digital circuits with low power consumption and long operation lifetime. The power dissipated in CMOS circuits has two components: static, due to leakage current, and dynamic, due to switching activity. The static power is relatively low and is often neglected in power estimation. The dynamic component of power which occurs only during transition of internal circuit nodes from one logic level to another is given by the following expression:

$$P = \sum_{i} V_{DD}^{2} C_L f E_{sw} \quad (1)$$

Where V_{DD} is the power supply voltage in CMOS logic, C_L is the load capacitance at node i , f is the frequency of operation of the circuit , $E_{sw}$is the power consuming switching activity at node i, (number of gate output transitions/clock cycle)[1-4].It is understood from the above expression of the power consumption ,for a given CMOS technology with specified supply voltage of the circuit design, switching E_{sw} of a node i is the only parameter that affects the power consumption[5],since it is dependent on the input pattern and the circuit structure. A method for calculating the switching for combinational circuits realized using gate logic was presented in [6], where the switching activity for a logic gate refers to the total number of 0 to 1 and 1 to 0 transitions occurring at the output of the gate while all possible two pattern input sequences are applied at the input of the gate. By using their definition the switching activity for a logic gate can be evaluated by the following expression,

$$A_T = \sum A_i = \sum_{i} 2 \left| F_i \right| \left| R_i \right| \quad (2)$$

Where ATis the total switching activity of the circuit, and A_i is the activity at node i. F_i represents the set of minterms of the logic function realized at node i and Ri represents the maxterms. $\left| F_i \right|$ and $\left| R_i \right|$represent the cardinality of the sets Fi and Ri respectively. The switching activity estimation by assigning an integer value as defined in [6] makes it almost impossible for comparing different circuits since there is no reference metric on which comparisons can be made .Even though [6] provides a method for reducing the switching activity ,it does not provide a formal procedure for the design of a combinational circuit with reduced switching activity .A disjoint implicant approach for reducing the switching activity was proposed in[7],that aimed at increasing the number of inputs to a gate. The partitioning of

the prime implicants of a minimal sum -of -products expressions that share minterms into disjoint implicants increase the number of inputs to a gate ,which directly reduce the switching activity by 10% with marginal increase in circuit area and delay. An algorithmic approach using K-map had been proposed in [3], which modifies the normal optimal solution obtained from K-map to reduce its switching activity providing for more than 10% reduction in switching activity. In this paper a synthesis approach for reducing switching activity of many combinational logic circuits depending on the truth table of the logic expression is proposed.

2. Switching Activity in CMOS Combinational Logic Circuits

To estimate the power consumption of a circuit with high accuracy, a large number of input signal patterns should be simulated and the average value of E_{sw}calculated [8]. Switching activity can be calculated by a probability propagation algorithm whereby the transition probability of an internal circuit node is calculated from the signal probabilities of the primary input variable .The signal probability can be represented as follow [9]:

There is a binary sequence x (of length l), where m bits are logic 1.Then the probability that the signal is measured as 1 in a random clock cycle is m/l, and one can denote:

$$P(x=1) = m/ l \quad (3)$$

Obviously, there is n-bits (n= L-m) which has logic 0 in the sequence. Therefore the probability that the signal is measured as 0 in a random clock cycle is n/ L ,and one can denote

$$P(x=0) = n/ l \quad (4)$$

Therefore $p_{0\rightarrow1} = n / l * m/ l$ and $p_{1\rightarrow0} = m/ l * n/ l$,where $p_{0\rightarrow1}$ and $p_{1\rightarrow0}$ are the transition probabilities of the outputs switching from 0→1and 1→0 respectively .But battery power consumed is only when the output switches from 0 → 1 so the switching activity of two input AND gate equal to 3/16 ,for inverter equal to 1/4 ,for three input AND gate equal to 7/64 and for four input AND gate equal to 15/256 ,from this it is clear that switching activity is maximum when the number of $1'S$ and $0'$ S of the function are equal .Since inverter has equal number of $1'S$ and $0'$ S in its function ,it has the highest switching activity and this

explain why one have to avoid input inverters in designing logic circuits. Switching activity of a gate is also a function of the number of inputs to the gate .

A gate with fewer inputs will have higher switching activity compared to a gate with more inputs .Hence increasing the number of inputs to a gate is also an important design consideration for combinational logic design for reduced switching activity.[3,7]

3. Design of combinational logic circuits with minimum switching activity

In this section a simple procedure is introduced for designing low power consumption logic circuit based on writing the truth table of the logic expression then comparing the minterms respectively in order to eliminate the complementary variable, then eliminate the same minterm if exist, compare the remaining variable to see if it is possible to eliminate the complementary variable if exist as shown in the two example below:

Example 1: **F=∑ 0,1,4,5**

A B C DA B C DA B C D

0 0 0 **0** 0 **0** 0 --- 0 --- 0 ---

0 0 0 **1** ⇒ ---------- ⇒ ⇒ - - AC

0 1 0 **0** 0 **1** 0 --- ----------

0 1 0 **1** ----------

Example 2: **F=∑ 0,2,4,6**

A B C DA B C DA B C D

0 0 **0** 0 0 **0** -- 0 0 -- -- 0

0 0 **1** 0 ⇒ ---------- ⇒ ⇒ - - AD

0 1 **0** 0 0 **1** -- 0 ----------

0 1 **1** 0 ----------

So one can get the simplified minterm with no need to draw the K-map.

4. Simulation results

1- $f_1 = \sum 1, 3, 5, 8, 9, 11, 13, 15$

$f_1 = \bar{a}\bar{b}d + bc\bar{d} + ab\bar{c} + acd$ **{using the proposed method}**

$= (a+b)d + b\,c\bar{d} + a(b+c) + acd$

3/16 1/ 3/1 7/64

7/64 7/64 7/64

1/4

Switching activity for this implementation is:

E_{sw} 1/4, 3/16, 7/64, 7/64, 3/16, 7/64, 7/64, 1/4

$f_1 = c\bar{d} + a\bar{b}\bar{d} + ad + ab\bar{c}$ **{ using k- map method }**

$= c\bar{d} + (a+b)d + ad + a(b+c)$

1/ 3/16 3/16 3/16

3/1 7/64 7/64

1/4

Switching activity for this implementation is:

E_{sw}=1/4, 3/16, 3/16, 7/64, 3/16, 3/16, 7/64, 1/4

There is about 10% saving in switching activity

2- $f_2 = \sum 0, 1, 4, 6, 9, 10, 12, 14$ **{ using the proposed method }**

$f_2 = \bar{a}\bar{b}\bar{c} + bd\bar{} + ab\bar{c}d\bar{} + ab\bar{c}\bar{d}$

$= (a+b+c) + b\,d\bar{} + ac(b+d) + ad(b+c)$

7/64 1/4 3/16 3/16

3/16 15/25 15/256

1/4

Total switching activity for this implementation:

E $_{sw}$=1/4, 7/64, 3/16, 3/16, 15/256, 3/16, 15/256, 1/4

f$_2$= ā b̄ c̄ + b d̄ + a c̄ d + b̄ c d̄ **{using the proposed method}**

= (a+ b + c) + b d̄ + a c̄ d + (b + d) c

1/4 1/4 3/16

7/64 3/16 7/64 7/64

1/4

Total switching activity for this implementation is:

E $_{sw}$ = 1/4,1/4, 7/64, 3/16, 7/64, 3/16, 7/64, ¼

There is about 11% saving in switching activity.

3 – f $_3$= ∑ 0, 1, 3, 4, 6, 7, 9, 12, 15

f $_3$ = ā b̄ c̄ + ā c d + ā b d̄ + a b c d + a b c̄ d̄ + a b̄ c d̄ **{ using the proposed method }**

= (a+b+c) + ā c d + (a+d) b + a b c d + a b (c + d) + ac (b+d)

7/64 1/4 3/16 15/256 3/16 3/16

7/64 7/64 15/256 15/256

0.2211 0.145

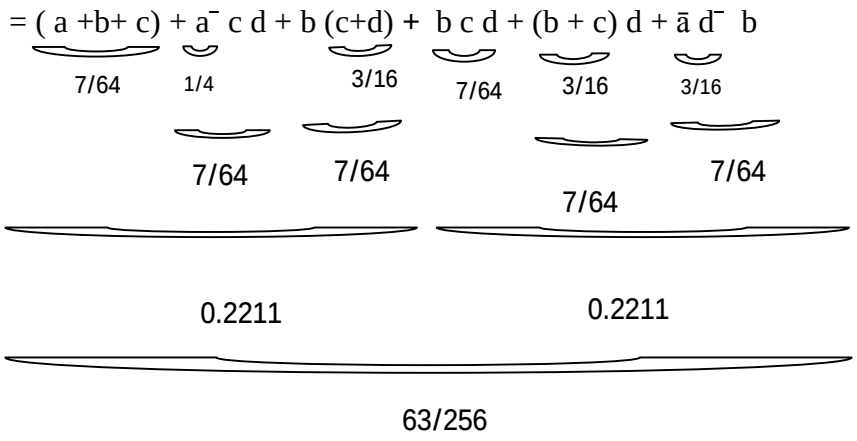
63/256

Switching activity using this implementation is :

E $_{sw}$= 1/4 , 7/64 , 7/64, 3/16, 7/64, 15/256, 3/16, 15/256, 3/16, 15/256, 0.2211, 0.145,

63/256

f $_3$ = a b̄ c̄ + a c d + b c̄ d̄ + b c d + b̄ c̄ d + ā b d **{ using k- map method }**



Switching activity using this implementation is :

E $_{sw}$ = 7/64, 1/4, 7/64, 3/16, 7/64, 7/64, 3/16, 7/64, 3/16, 7/64, 0.2211, 0.2211, 63/256

There is about 11% saving in switching activity.

5. Conclusions

In this paper a synthesis approach for the design of combinational logic circuits, with the primary objective of minimizing their switching activity is introduced. This paper shows clearly that there is no need to draw the k- map and to decide which group of minterms will be selected and which group will give the less switching activity, since from the truth table one can directly write the simplified equation which will give the optimum switching activity, the results shows that about 10% saving in switching activity is obtained using this procedure.

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